oregon magnetics

VS-1000

Service and Operation Manual

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PCBs

SECTION 1

SETUP AND OPERATION

1-1 CONTROLS

1-2 Panel Switches

POWER on-off: Instantly turns on all VS-1000 functions except its 110 V output to power VCR. There is a 30 second delay before output power is available.

PRESET-SERVO: In PRESET mode the VS-1000 is a fixed frequency power source, there is no servo action. The output frequency is accurate enough to properly operate any VTR/VCR.

MONITOR-DISPLAY: Affects only the MONITOR output. In the DISPLAY position it adds REFERENCE SYNC to the VTR playback video creating a display of the VTR speed and stability.

1-3 Lamps

PILOT: Lights anytime VS-1000 is turned on.

INPUT: Lights when either or both video (or sync) inputs are missing.

PRESET: Indicates when the VS-1000 is in the PRESET mode (i.e. no servo action). This is automatic if one or both inputs are missing. A modified VCR will set the PRESET mode whenever it is not in the PLAY mode.

LOCK: Lights whenever the servo is more than ± 1.5 lines out of lock. (The LOCK PHASE control shifts this detector along with the lock phase.)

1-4 Adjustments Behind Door:

LOCK PHASE: Adjusts the relationship between tape playback and reference sync or video.

FREQUENCY: Useful only in the PRESET mode (except for setup testing). This allows a speed change of approximately $\pm 5\%$ from nominal (± 3 cps at 60 cps). It is useful with AF recorders and establishing lip sync between recorders.

1-5 Test Points Behind Door

REFERENCE GROUP: Derived from REFERENCE input.

VIDEO: Buffered low pass filtered video.

SYNC: TTL compatible stripped composite sync.

SQUARE: 60 cps square wave, rise triggered by vertical sync.

ADVANCE: 60 cps negative pulse. Fall is 5 lines before vertical sync, rise triggered by vertical sync.

1-6 VTR GROUP: Derived from CONTROLLED VTR VIDEO

VIDEO: As above.

SYNC: As above.

SAMPLE: Servo sample pulse. 30 μs positive pulse approximately 15 lines after vertical sync.

1-7 NOT GROUPED

MONITOR: Same as MONITOR output at rear panel.

ERROR: Phase detector error voltage. Normally at +5v d.c. Varies at the rate of 180 mv. per line of error.

TEST BUTTON: Causes a 2 line change in lock phase when held in. Used for checking servo/VCR set-up.

1-8 SET-UP

1. Make a 15 minute recording on the VTR or VCR to be used with the VS-1000. Power the VTR from the local power line not the VS-1000.
2. Set the VS-1000 switches as follows: MONITOR, PRESET, OFF.
3. Feed the video output of the VCR to the VS-1000 CONTROLLED VTR VIDEO (either connector, they loop through).
4. Feed house sync to the REFERENCE SYNC or COMPOSITE VIDEO connector (another loop through).

   Note on 3 & 4: The 6 pin DIN connector can supply these signals from the VCR, if the VCR is so equipped.

5. Hook up a monitor to the MONITOR connector.

6. Turn on VS-1000 - the PILOT, LOCK, and PRESET lights should come on and the output of the VCR should appear on the monitor. If either the house sync or CONTROLLED VTR VIDEO is not present, the INPUT light will light.

7. Play back the tape made on that VCR, still powered from the local power line.

8. Set switch to DISPLAY. This will add house sync to the output of the VCR on the monitor, causing a display of VCR video stability and frequency compared to house sync. The frequency should be close since the tape was just recorded. Study the speed changes, jitter, etc.

9. Unplug VCR from the local power line and plug into the POWER FOR VTR outlet.

10. Again play the tape. A similar display should result, but there may be some speed difference due to the servo output being at a slightly different frequency than the local power line.

1-9 SETTING OF THE RESPONSE TIME

1. Open the door by turning the knob $\frac{1}{4}$ turn counterclockwise.

2. Start with the very slow setting of LOW PASS = 9, GAIN = 2.5, RATE = 0, and DAMP = 0.

3. Power the VCR from the servo.

4. Set switches as follows: MONITOR, PRESET, ON.

5. Set VCR to play.

6. Set monitor switch to DISPLAY after a picture appears.

7. Verify that VCR is running close to proper speed (i.e. more than 3 sec for the vertical blanking to roll through the picture).

8. Set servo to the SERVO position. The VCR should slowly v-lock. Its jitter and random speed changes will be apparent.

9. Push TEST button and hold in. The picture will slide sideways about 2 lines (if this isn't enough to plainly see, set LOCK PHASE fully clockwise and pull out, the test jump will now be 5 lines). Release TEST button after picture comes to rest.

   a. If at any time the servo should get far off speed, it may

be rapidly brought back to 60 cps by the following:

i. Set to PRESET.
ii. Rotate LOW PASS to zero and hold for 1-2 seconds.
iii. Return LOW PASS to previous setting.
iv. Correct whatever made it go offspeed.

10. Alternately push TEST (hold in until picture comes to rest, then release) and advance GAIN control about 1 division at a time until overshoot is apparent. Back off to the point where there is little or no overshoot. Do not be confused by the natural back and forth motion of the VCR output.

11. Using the same procedure gradually reduce LOW PASS until overshoot is apparent.(this time overshoot is very slow). Set as low as possible without overshoot.

12. This setting will keep a good VCR within a $\pm 1\frac{1}{2}$ line window, but a good safety factor makes a faster action desirable.

13. Alternately push TEST and advance RATE as you did with GAIN. This will speed up the response to your jump. Advance it until some oscillation becomes apparent on the jump. Set it for the fastest response <u>without</u> oscillation.

14. Repeat for DAMP control (here the oscillation will be very fast and may appear as jitter). Here you may notice a rapid jump followed by a slower drift in the same direction. In that case advance GAIN to eliminate this slower portion of the jump. A rapid jump followed by very slow overshoot indicates that the LOW PASS is set too low.

15. If required, the LOW PASS can be reduced at this time to counter slow drifting of VCR. Once again avoid overshoot. A good test at this point is as follows:

    a. Set to PRESET.
    b. Pull out FREQUENCY adjust and adjust manually to set tape vertical about 1/3 way down from top of screen.
    c. Push off FREQUENCY.
    d. Set to SERVO. This will show lock-up behavior and will indicate how far you can reduce the LOW PASS.

16. The final result should be a response that, when tested, will jump rapidly and come to a smooth rapid stop without overshoot or jitter. This is a good setting for general purpose TBC use.

17. The VS-1000 can be adjusted for a wide variety of response characteristics. The foregoing should be considered a quick way to get a good set up for any one VTR, not the only usable method or settings. Some other responses are noted below.

18. Bad tapes or VTR's may require advancing all controls slightly to get minimum peak to peak drift in order to stay inside a window. This is best done by watching the stability display while slowly advancing GAIN, RATE, and DAMP, and retarding LOW PASS.

19. Conversely to play tapes without a TBC (i.e. to give interlaced color off of all tapes) over a cable system or for dubbing, it is desirable to guarantee that there is no increase in jitter by reducing the response speed to the point of zero overshoot or slower. This is mostly true of the RATE and DAMP controls as they can increase jitter if advanced too far. It should be noted that some TBC's will let through some jitter. Dropouts can affect the lock. A slow response is very immune to dropouts.

20. Slow settings are very stable in the long term, while fast settings become a critical balance, and will drift as VCR warms up, etc.

1-10 TYPICAL RESPONSE SETTINGS

For optimum performance follow the set-up procedure given in 1-9. The following can serve as a guide to usable settings for various VTRs.

	L.P.	Gain	Rate	Damp
Sony AV 3600 O	7.0	4.5	5.5	6.5
Sony CV 2000	4.5	5.2	4.2	5.0
Panasonic NV 3020	6	5	4.5	4.5
JVC CR 6000	6.5	5.7	6.2	6.6
Audio Recorder	4	6.2	0	0

SECTION 2

INTRODUCTION TO THEORY OF OPERATION

2-1 MAIN CIRCUITRY:

2-2 The VS-1000 is comprised of 8 basic functions contained on 7 printed circuit boards (PCB). What follows is a brief functional description of the unit. The next section (2-13) will detail each circuit by PCB.

2-3 The two video inputs are applied directly to their sync separators. These are especially designed to handle the sometimes poor sync from inexpensive helical VTRs, and give clean sync out with as little as 30% of normal amplitude at the input. The composite sync stripped from both inputs is applied to a pair of vertical integrators which separate the vertical sync. The house sync vertical integrator is processed first to a square wave, then into a linear ramp of about 2 ms duration.

2-4 The VTR vertical integrator's output is used to derive a 30 μs sample pulse. This pulse causes an electronic switch to close for 30 μs, then reopen, connecting the linear ramp to a storage capacitor. The relative timing between the ramp and sample is reflected in the voltage on this capacitor. Thus the voltage is an accurate measure of the timing error between the VTR and the house sync. The storage capacitor's voltage is processed, then applied to the voltage controlled oscillator operating at a frequency of 9.6 KHz.

2-5 This is divided by 160 and processed to provide a 3-5-3-5 timing sequence. This is a 3 level approximation of a sine wave which is applied to the switching mode power amplifier. The output is voltage regulated and current limited.

2-6 AUXILIARY CIRCUITS:

2-7 LOCK indicator: This delays the leading edge of the square wave derived from house sync, forms a window, and then checks whether the sample pulse is within the window. If it is not, a .2 second one shot causes the LOCK LED to light.

2-8 INPUT fault indicator: This checks for presence of both square wave derived from house sync and the sample pulse derived from VTR video. If either is missing continuously for $\frac{1}{2}$ second, the INPUT LED lights and the VS 1000 is automatically switched to the PRESET mode.

2-9 PRESET mode: When the PRESET mode is selected, either manually

or automatically, the VS 1000's servo action is disabled and it becomes a fixed frequency power source of high accuracy and stability. The points of control are inhibition of the sample pulse and clamping of the storage capacitor to nominal voltage. The action is a smooth transition with no jumps or glitches in the 60 Hz output frequency. The PRESET mode may be selected in any of three ways:

1. the front panel switch.
2. a loss of either video input for more than ½ second (See INPUT fault indicator above).
3. through the two control lines connected to the 6 Pin DIN connector located on the back panel.

2-10 Stability DISPLAY and MONITOR output: The MONITOR output is derived from the VTR input and is meant only for a monitor, as it is subject to some interference. Its real value is when the switch is put in the DISPLAY position. House sync is then added to VTR video and the monitor shows all instabilities in the VTR.

2-11 TEST button: This is wired across ½ of the LOCK PHASE control, and causes the LOCK PHASE to shift by 1½ lines. Its purpose is to shock the VTR, showing the dynamic response of the VTR/VS 1000 combination when finding the settings for a new VTR.

2-12 Delayed Turn On: When the VS 1000 is turned on, the very large power supply capacitors would draw excessive surge current. Therefore a resistor is used as a limiter and a relay bypasses it after a reasonable time delay.

2-13 DETAILED THEORY OF OPERATION

2-14 Sync Separator PCB. This PCB contains two sync separators and the monitor buffer/display generator.

2-15 Input video is applied directly to U1B, an emitter follower isolation stage (U1 and U2 are each 5 NPN transistors contained within one IC). This isolated video goes to the front panel test point as well as the AGC stage comprised of R6, R7, and U1E. The resultant constant level video is applied to a partial sync separator U2C. The positive going sync tips at the collector of U2C are clamped by the feedback action of U2A with C4. R8 provides the discharge time constant, and R9 limits the charging current. C5, R11, and U2B (diode connected) provide transient clipping which prevents VTR head switch glitches from upsetting the AGC circuit. An emitter follower (U2D) provides low impedence drive to the sync separator which follows.

2-16 The signal at this point (TP-1) has a positive sync whose tips are clamped at 2.25 volts. Some video remains, depending upon input level. Back porch will typically be at .85 volt with 1 volt P-P video input, and will vary with input level. U2E is the actual sync separator and is biased to slice at the midpoint between back porch and sync tip. Its output (TP-2) is TTL level and drives one inverter (U3A). The output of U3A drives 3 inverters and the back porch circuit. One inverter (U3E)

drives the vertical integrator, one (U3D goes to the front panel test point, and the last (U3F) is an open collector sync tip clamp for the monitor buffer.

2-17 U3B, R22, and C7 detect the negative going trailing edge of sync. R24 and C8 provide a short delay at the input of U3C, the back porch clamp. U1A buffers the video from the sync tip clamp before U3C clamps the back porch. This gives positive going sync with the back porch always at 0 volt and a tip amplitude which varies with video input level. The sync level is then peak rectified by U1D and C10, which serve as the AGC detector. This DC voltage is then applied through R27 to U1E, the AGC control element.

2-18 Monitor Buffer/Display Generator

2-19 Input video from buffer U1B is applied to emitter follower Q1 after being sync tip clamped by U3F. Thus the base of Q1 has sync tips at 0 volt DC and the emitter has them at +.6 volt P-P video. A clamp at the emitter of Q1 pulls this point to 0 volt for insertion of house sync on the monitor output yielding the stability display. This second clamp is U3F of the reference sync separator, and is selectively applied through the DISPLAY switch.

2-20 Vertical Sync Separator PCB

2-21 Negative going composite sync is applied to the vertical integrator R1C1, R2,C2, and R3C3, where it emerges as a negative pulse. This triggers U1, a 9 ms one shot whose output is a 60 Hz square wave that eventually becomes the ramp signal. U1's output also triggers U2 and U3. U2 is a 16 ms one shot which inhibits the input of U1 for 16 ms (almost one full field) after each vertical sync pulse. This provides good noise immunity.

2-22 U-3 is triggered by the end of U1's 9 ms pulse. U3 is adjusted to last until .4 ms after the next vertical pulse. Thus one of those is normally always in the triggered state. If a house sync vertical pulse were to be missing, then .4 ms later both U1 and U3 would be untriggered. This condition is sensed by NAND gate U4C and is used in the Logic PCB to immediately stop the next sample pulse.

2-23 R12 C11, R13 C12, and R14 C13 form the vertical integrator for the VTR sync output of the sync separator. U5, a one shot, is triggered by this vert pulse and provides an adjustable delay between tape vert sync and the sample pulse. Since the servo is a feedback loop which always keeps the sample pulse at a fixed point on the ramp, a control on U5's delay effectively varies the lock up phase (or timing) between the VTR and reference.

2-24 U7 is a 30 s one shot triggered by the end of U5's pulse. This is the sample pulse. U6 is a noise immunity one shot similar to U2, except that R20 and D3 cause its output pulse to shorten when the VTR is not in lock.

2-25 Logic PCB

2-26 U1-U3 form the lock up detector whose purpose is to light the indicator LED and shorten the period of the noise immunity one shot on the vert sync PCB when the VTR is not in lock. The 60 Hz square wave's leading edge is delayed by U1. U1's trailing edge triggers U2, the window pulse generator of 220 s duration. This is applied along with the 30 s sample pulse to U3's input logic. The operation of U3's input is such that U3 is not triggered if the sample pulse is entirely within the window. If the sample pulse overlaps or falls outside of the window, U3 is triggered , lighting the LOCK LED and adjusting the noise immunity. (1-24)

2-27 U4A and U6 comprise the no input detector. When either input of U4A is a logic 0, R7 will charge C4 towards 5 volts. Normally the sample pulse of 30 s at a 60 Hz rate will keep C4 at approximately 1.4 volts. The other input to U4A is from the missing vertical detector on the vert sync PCB, which is normally at a logic 1. The R7 and C4 time constant is such that U6 triggers after about .4 seconds of either video input being missing. This lights the INPUT LED and selects the PRESET mode by grounding the "open collector" preset buss.

2-28 When either the missing vertical sync detector on the vertical sync separator PCB or the preset buss goes to logic 0, U4C's output goes to logic 0 and inhibits the sample pulses at U4D. The output of U4D directly drives the sample transistors on the phase detector PCB.

2-29 When the preset buss is at a TTL logic 1, servo action is permitted. When it is at a logic 0, servo action is inhibited and the VS 1000 becomes a fixed frequency 110v AC power source. R10 keeps it at a logic 1 unless one of the following pulls it to logic 0:

1. no input detector, U6
2. "1 = Record" input, U5A.
3. "1 = Run" not being present and 6P DIN pin #6 is jumpered to ground, U5B and U5C.
4. front panel PRESET switch.

The preset line is level shifted to 10 volt logic for the phase detector PCB by U5D and U5E.

2-30 Phase Detector PCB

2-31 This PCB accepts the 60 Hz square wave and 30 μs sample pulse, compares their timing, and derives a 9.6 KHz signal proportional to their time difference.

2-32 U1 and Q1 provide a ramp which linearly falls from 5 volts to approx. 0 volts. U2 level shifts and inverts this ramp. U1D and E provide a constant current discharge for C1. U1A (diode) provides the proper relationship between ramp slope and the +5 volt supply. U1C charges C1 under the control of R7, Q1, and the input 60 Hz square wave. U1B (diode) serves to cancel the base-emitter voltage drop of U1C.

2-33 U2 is a unity gain inverter with its reference input set by R9 and R11 to level shift the ramp without affecting its amplitude. Its output (TP-2) is a 5 volt P-P linear ramp centered about the 5 volt supply (ramp rises from +2.5 volt to + 7.5 volt).

2-34 Q2 is a PNP transistor used as a SPST switch. It samples the ramp from U2 by charging C3 to the instantaneous ramp voltage. Q3 sets C3 to +5 volts when in the PRESET mode. U3 is a follower to avoid the loading of C3 by the circuits which follow. TP-3 and the front panel test point are taken from the output of U3.

2-35 In order for a servo to be accurate, the gain must be high, but high gain produces stability problems. The usual procedure is to provide as much gain as possible without oscillation, then provide even more gain at very low frequencies. The GAIN control sets this overall gain, while the LOW PASS control sets the frequency (with C4) at which the gain increases by about 15-20 times. This is sufficient for acceptable servo action, but the requirements of helical make a faster action desirable. Q5 and U4 form a rate of change detector whose output is added to the error signal in order to speed up the overall VTR/VS-1000 response. C8 and the DAMP control differentiate the rate signal and serve to prevent high frequency (about 10 Hz) oscillation as the RATE control is advanced.

2-36 R20 and C6 form a delay circuit for the error signal. C7 couples this delayed signal to U4 with clamp Q5 setting it to DC reference just before the next sample arrives. The result is a signal whose amplitude is the difference between the previous sample and the current one - a true rate of change. U4 is a gain of 4 buffer whose output (TP-4) is the RATE control. C8 differentiates the leading edges of this signal to provide a damping action, allowing the RATE control to be set higher without oscillation.

2-37 U6 sums the 4 error signals, each weighted so that its control will be approximately centered with a "typical" VTR. C9 removes residual noise while R32 and R34 level shift U6's output (centered about +5 volts) to match U8's FM input (centered about 3.3 volts).

2-38 U8 is a standard multivibrator using very stable components (R40, R41, R42, R43, and C12). If standard components are substituted here, the output frequency will not be stable in the PRESET mode. U7 is a temperature compensation circuit used to further stabilize the circuit. R35, 36, and 37 form the stable arm of a bridge, while R39, U7D and U7C form a temperature varying arm. R38 allows the selection of any temperature coefficient between stable and 2 diodes. U7B cancels one diode so that R38 effectively selects one diode of positive through one diode of negative temperature coefficient.

2-39 The output of U8 is a rectangular TTl signal with a constant width low portion, and a variable high portion. This goes to the power driver PCB.

2-40 Power Driver PCB

2-41 The power driver PCB receives the 9.6 KHz signal from the phase detector PCB and provides a 3-5 symmetry 60 Hz drive at approximately 1 watt to the high voltage switching transistors on the power output PCB. It also contains voltage regulation (section 2-45), current limiting (section 2-47), low line voltage detection (section 2-48). and delayed turn on circuitry (section 2-48).

2-42 The FM signal at 9.6 KHz is applied to U1, a ÷10 with a 960 Hz symmetrical square wave output (TP-1). U3 further divides this by 8, yielding 120 Hz (TP-3). U6A uses various outputs of the previous dividers to provide a 3-5 waveform. The 120 Hz square wave (TP-3) is applied to U6A's input. The leading edge is delayed by 1 ms ($\frac{1}{2}$ cycle from the 960 cps ÷ 2) by clocking (rise triggered) U6A from U3's ÷2 output (TP-2). This delay results in the required time sequence of 3-5-3-5 (TP-4).

2-43 U6B is clocked at 120 Hz from U6A's Q output, then reset $\frac{1}{2}$ms later by the 960 Hz square wave from U1. This (TP-1) is applied to U3's last stage (a ÷2) to yield a 60 Hz square wave which selects the polarity of the output (TP-11 and TP-12). It also unconditionally turns off the output drive to allow a slight gap between negative and positive output drive (Q output, TP-5).

2-44 A "0" at any input of U8A will turn off output drive. This can be:

1. TP-5 above 2-43.
2. the 3-5 wave form except for pull down purposes (section 2-46).
3. excessive output current (section 2-47).
4. the output voltage being too high (the switching regulator has only two states: too high, too low).

U8B, U9A, and U9B form a two phase drive with non-overlappingedges. This is logically gated with a 60 Hz drive select to drive Q1 through Q4 connected in a bridge configuration. U17, a full wave bridge, provides transient clipping at a primary of the drive transformer.

2-45 U12 is the voltage regulator comparator. One input is the 3-5 waveform from U6A, the other is from the optical isolator on the power output PCB. R13, R14, C1, and U10E translate U6A's output to TTL (TP-6). Since the optical isolator's output is a current, R9 provides a means of setting the isolator's gain, and hence the output voltage. R11, R12, D1, D2, and C3 provide a one shot action to establish a minimum off time and therefore an upper limit on the switching frequency.

2-46 Normally, only one output transistor can be on during any $\frac{1}{2}$ cycle of the 60 Hz output. However, with capacative loads (or no load), the output voltage will not fall to 0 during the 3 units time between output power pulses. U7A detects this condition and prematurely enables the opposite polarity through U2C and U2D. The trailing edge of U6B's $\frac{1}{2}$ ms pulse (TP-5) samples the output voltage by clocking U7A. If the

output voltage has not fallen almost to 0, U7A will clock, enabling output drive (through U2C) just after polarity changes, to pull the voltage to 0. If it was 0, or when it reaches 0, U7A will be reset by U10E (TP-6) from the voltage comparator. (TP-6 is high when the output voltage is too high.)

2-47 U11 is the current limiter comparator and is similar to the voltage comparator, except that its reference is a DC voltage. Its translated output resets U7B, which causes the drive to be shut off at U8A. This flip-flop is normalized by clocking in a "1", which can occur at a maximum rate of 9.6 KHz.

2-48 U10A and U13 provide an initial turn on delay and low line voltage protection. C6 and R25 determine the delay, while U10A will discharge C6 if D3's cathode (the 10 volt power supply) falls below 9 volts. U13 serves as a level detector and Schmitt trigger with 1.67 volt hysteresis. Q5 is the relay driver. R28 and C8 insure that there is a short delay between the relay pull-in and application of drive to the output transistors. U10C and U10B inhibit drive to the output transistors by shorting the base drive to two of the four drivers, Q3 and Q4.

2-49 The power transformer secondary, 24 volt ct, is rectified by D6 and D7, and filtered by C10. U16 and U15 regulate this at +5 volts and +10 volts respectively. Note that U16 is the reference for U15, permitting the use of identical regulators.

2-50 Power Output PCB

2-51 NOTE THAT C5 AND C6 HOLD ENOUGH ENERGY TO MELT TOOLS OR GIVE A DANGEROUS SHOCK. ALWAYS DISCHARGE BOTH C5 AND C6 WITH A 1K 2W RESISTOR FOR AT LEAST FIVE SECONDS BEFORE WORKING ON THIS PCB.

2-52 Q1 and Q2 are the line voltage switching transistors. They alternately connect the +150 and -150 volt supplies to the output through lowpass filter L1, C2 and R10.

2-53 Q1 and Q2 should be considered as common emitter, saturated switches, since base drive is connected between base and emitter and is not referenced to ground. R1 and R3 help smooth out the load on the driver transformer, while R2 and R4 reduce drive current dependency on transistor characteristics.

2-54 Either R5 or R6 is in series with the load, depending upon which transistor is conducting. The voltage across them is proportional to transistor current and is sensed by optical isolator U2 for current limiting purposes.

2-55 D1 and D2 clamp inductive spikes to protect Q1 and Q2.

2-56 The full wave bridge U3 rectifies the output voltage for voltage regulation. R8, R9, and C1 provide current limiting and proper dynamic response for the voltage regulation optical isolator U1. These are a high speed type isolator, and should not be substituted.

2-57 R14 limits initial charging current for C5 and C6. After about 10 seconds, the relay pulls in (Section 2-48) and shunts R14 with R13. D3 and D4 each half wave rectify the power line voltage to supply +150 volts and -150 volts for Q1 and Q2. R11 and R12 are bleeders to discharge C5 and C6 when the VS-1000 is off. C3, C4, and C7 are RFI reduction components. Note that the heat sink acts as an RFI shield since it is grounded by C7 to the neutral side of the power line.

SECTION 3

MAINTENANCE

3-1 Service Hints

3-2 It is convenient to supply 1v P-P video to one input, then jumper to the other. This way both sync separator circuits have identical inputs and can be compared.

3-3 The Phase Detector PCB has several op amps which use a 0 and 10 volt power supply. The +5 volt supply is the common one for these op amps.

3-4 The VCO and associated components are very stable. Therefore any off frequency problems are indicative of component failure rather than normal drift. Check TP-7 for 5 volts $\pm\frac{1}{2}$ volt in PRESET, and U8 Pin 5 for 3.3 volts and P8-8 for the same voltage as TP-7.

3-5 When trouble shooting the VS-1000 it is good practice to unplug P-19, the driver transformer primary, and P23, the 110 volt AC input to the Power Output PCB, if possible. This will prevent damage to the transformer and/or power transistors in the event of accidents.

3-6 Base current to the H.V. transistors can be checked across R2 and R4 but BE SURE TO UNPLUG P-23, the 110 volt input to the PCB, AND DISCHARGE C5 and C6. Normal base current is .8-1.0 Amp for the DTS-709.

3-7 to 3-20 Vacant

3-21 ALIGNMENT

3-22 Test equipment required:

Dual trace triggered sweep scope
DC voltmeter capable of .1 volt full scale
Source of video or sync
Frequency meter or stable local 60 Hz power line
True RMS AC voltmeter

3-23 Set the VS-1000 controls as follows:

SERVO mode	
LOCK PHASE	push in
FREQUENCY	push in
LOW PASS	midscale
GAIN	midscale
RATE	midscale
DAMP	midscale

3-24 Connect 1 volt P-P video to either video input, loop through to the other input.

3-25 Sync Separator PCB

3-26 Check both TP-2s on the sync separator PCB for composite sync. Tips should be 0 - .3 volts, high level = 4.5 - 5 volts.

3-27 Vertical Sync Separator

3-28 Check both TP-1 and 3 on the Vert Sync Sep PCB for integrated V sync.

3-29 (Vertical hold off) Connect channel 1 scope probe on TP-2, channel 2 on P3-1. Trigger from channel 1 on (-). Adjust R10 so that the falling edge of TP-2 is 7 lines before the start of V sync.

3-30 (Vertical hold off) Move channel 1 probe to TP-4 and adjust R21 as above for R10.

3-31 (60 Hz symmetry) Connect a DC voltmeter between TP-2 and the 5v supply on the phase detector PCB. Adjust R5 (V sync separator PCB) for 0 .1 volt.

3-32 (Missing vertical detector) Connect scope to TP-7 and TP-5, trigger from TP-7 (+). Adjust R8 so that TP-5 falls 400 m s after TP-7 rises.

3-33 (Lock phase - preliminary adjustment) Connect DC voltmeter between TP-3 on the Phase Detector PCB and +5 volts. Adjust R16 for 0 ± .05 volt.

(see section 3-41 for final adjustment proceedure)

3-34 Logic PCB

3-35 (Lock Detector) Connect scope to TP-1 and TP-2, trigger from TP-1 (+). Adjust R1 to center 30 μ s sample in the 220 μ s window.

3-36 Phase Detector PCB

3-37 (Output frequency) The only adjustments on the Phase Detector PCB are the output frequency and temperature compensation for same. These circuits are very stable and should require adjustment only in the event of parts replacement. A touch-up may be desirable after several years of use.

3-38 If a digital frequency is not avaliable, and the local power line is stable (all of U.S.A.), a dual trace scope may be substituted as follows: Trigger from and display the 60 Hz power line on one trace, and the output drive on the other. (It is convenient to use the AC side of D1 or D2 on the 5 volt supply PCB and the driver transformer primary at P19-1 or 2 since both are accessible with the VS-1000 upside down.) Then any frequency drift will be evident by horizontal movement of the output drive wave form. Its frequency can be measured by timing the length of time it takes to move one complete cycle - 1 cycle in 5 sec = 1 cycle/5 sec = .2 cycle/sec. The permissible limits are ± .1%, which is 1 cycle in 16.7 seconds at any temperature. In practive, .05% can easily be set and maintained over long lengths of time.

3-39 The output frequency limits are designed to properly run a VTR with the VS-1000 in the PRESET mode. This is the worst case. These limits are:

1. Output 60 Hz ± .1% (16.7 sec or more for one cycle frequency drift)
2. At the VCO: 9.6 KHz ± .1% = 9591 to 9609 Hz

3-40 Let the VS-1000 fully stabilize at a room temperature of 65-75 F, then proceed as follows:

1. Put VS-1000 in the PRESET mode.
2. Rotate the LOW PASS control fully counter clockwise, then return it to the midscale.
3. Wait five minutes for C4 to charge up to U5's offset voltage before making any adjustments.
4. Check TP-7. It should be 4.5-5.5 volts; if not, circuitry trouble is indicated.
5. Connect a frequency meter to TP-8 or dual trace scope as in 3-38 above.
   If only a touch-up is desired ($\pm\frac{1}{2}$ Hz), adjust R41 (coarse) and R40 (fine).
   If components have been replaced then a full alignment will be required.
6. Set R38 fully clockwise.
7. Using fine (R40) and coarse (R41) frequency controls, set the output frequency at 60 Hz (9600 Hz at TP-8).
8. Rotate R38 fully counter clockwise, and then adjust R35 so the output frequency is 60 Hz (9600 Hz at TP-8).
9. Repeat 6-8 until the output frequency is correct at any setting of R38. Leave R38 at mid rotation.
10. Run a 100 watt lamp for two hours with the heat sink ventilation blocked, feeling the top cover occasionally to detect overheating (which should not occur).
11. Remove the bottom cover. Quickly reconnect the frequency meter and adjust R38 (temperature comp) to bring the output back to 60 Hz (9600 Hz at TP-8). This must be done before significant cooling of the Phase Detector PCB can occur.
12. Let the VS-1000 cool to room temperature and recheck output frequency, but do not adjust.

3-41 (Lock Phase - final adjustment)

1. Set the VS-1000 to PRESET.
2. Rotate LOW PASS fully CCW.
3. Measure the voltage from TP-7 to the +5 volt supply.
4. With the same video at both inputs to the VS-1000, set it to SERVO.
5. Adjust R-16 (Vertical Sync Separator PCB) so that TP-7 measures the same in SERVO as it did in PRESET to an accuracy of ±10 mv.

3-42 Power Driver PCB

3-43 (Output voltage) Connect an RMS voltmeter and a 100 ohm, 200 watt resistor to the 110VAC output, and adjust R9 for an output voltage of 110 volt RMS.

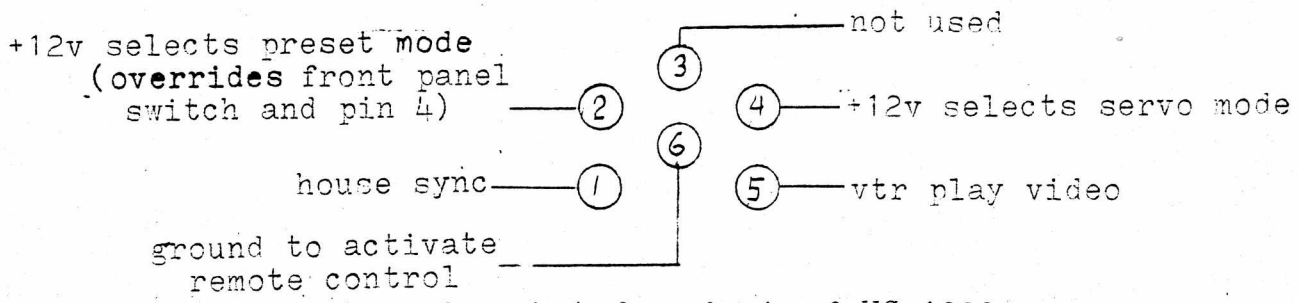
3-44 (Current limiting) Connect a 100 Ω 200 watt resistor, in parallel with a 1k 20 watt switchable resistor, to the power output. Connect a scope to TP-13; trigger from TP-12. Adjust R18 so that some negative pulses are evidenced with both resistors in parallel but none with only the 100 Ω resistor.

Hook-up of the 6P DIN (optional).

USE: In some set-ups it is necessary for the VTR to put out a video signal other than from the tape in standby, record, FF, or rewind. The VS-1000 will attempt to lock these signals by varying the 60Hz output frequency which may produce an off frequency recording or slow down lock-up when play is pressed. A control wire to the VS-1000 solves this problem.

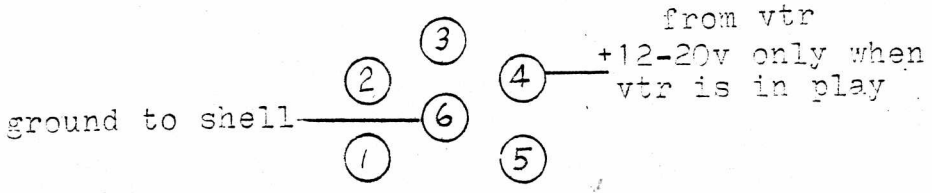
PARTS REQUIRED: 1-Switchcraft 12BL6M; wire; VTR end connector (optional).

HOOK-UP: The VS-1000 contains control input lines which activate the servo function only on command:



view of socket from back of VS-1000

We suggest the following wiring for this purpose:



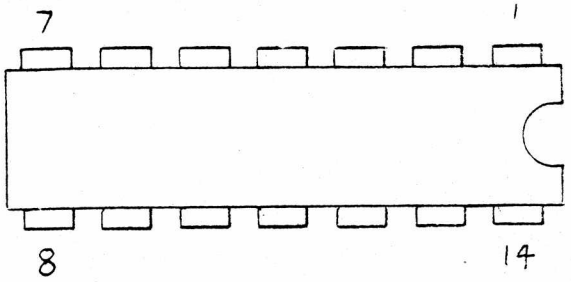
back view of plug

It may be desirable to have video also come in this connector for quick change purposes. Due to the sensitivity of the VS-1000's sync separator, 1-2V P-P from the VTR may be isolated with a 1K resistor and fed through a short length of unshielded multiconductor wire to this connector. This will somewhat load the video and if quality suffers, simple transistor buffer(s) will be necessary. Usually the video output stage will accept this 1K load if it is placed before the 75ohm source termination resistor.

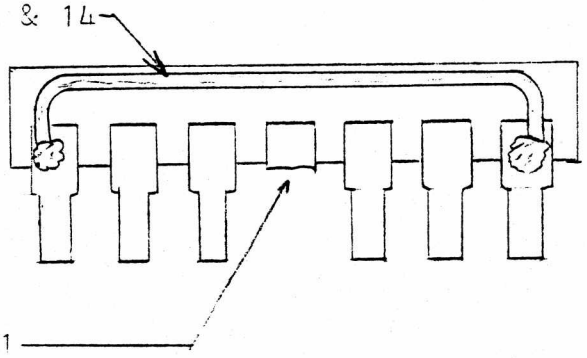
MODIFICATION OF THE VS-1000 FOR 50 Hz OUTPUT

Power driver PCB

Remove U1 (7490) and replace it with a 7492 modified as follows:

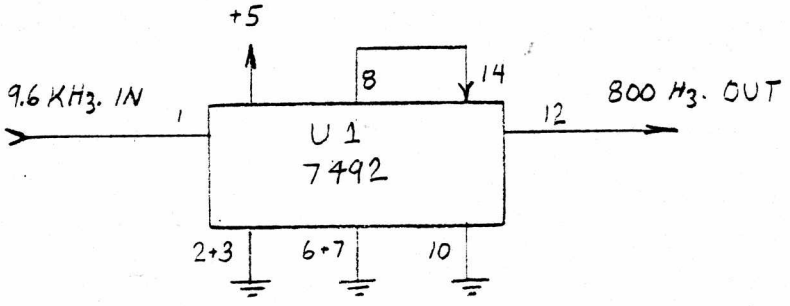


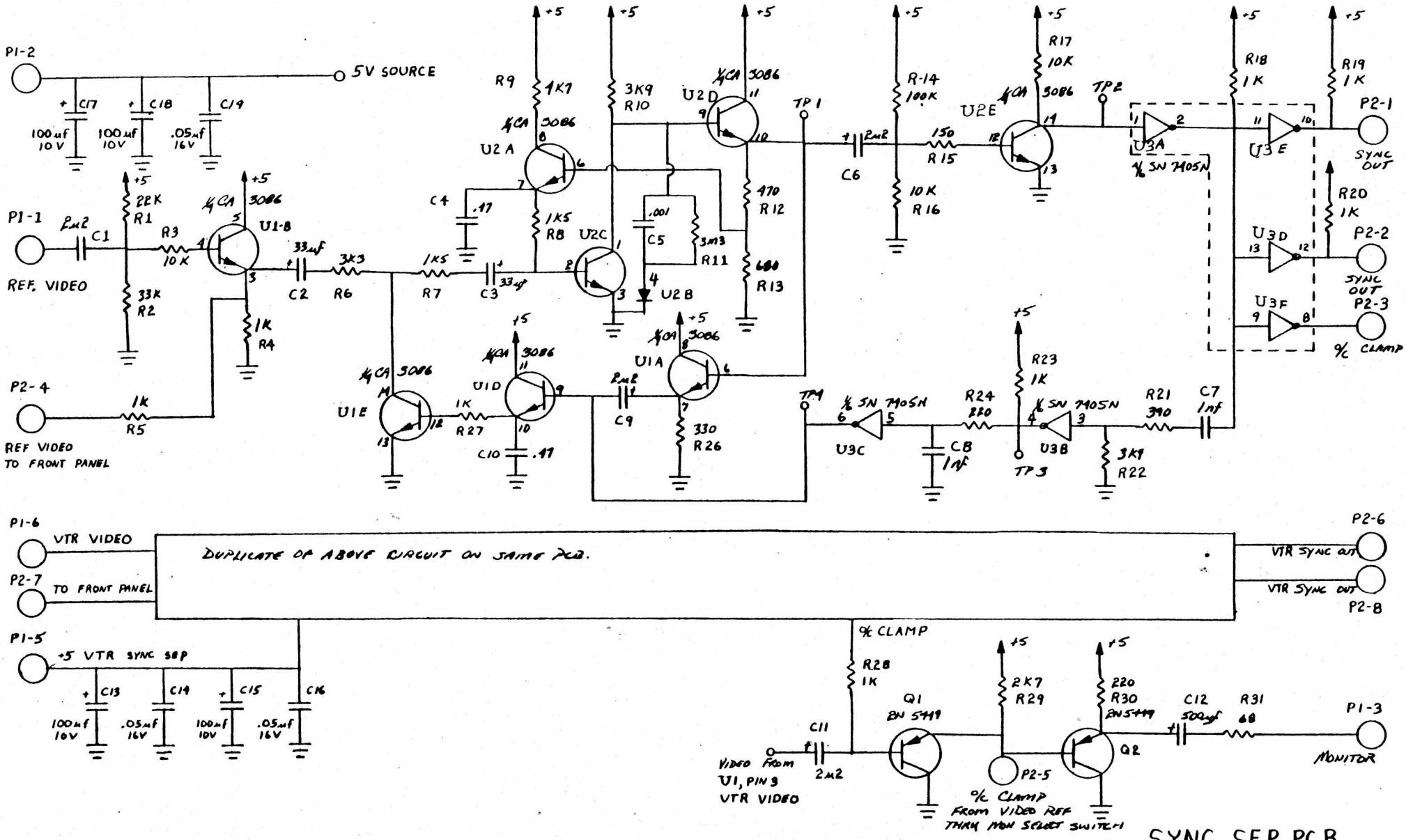
1) Jumper pins #8 & 14

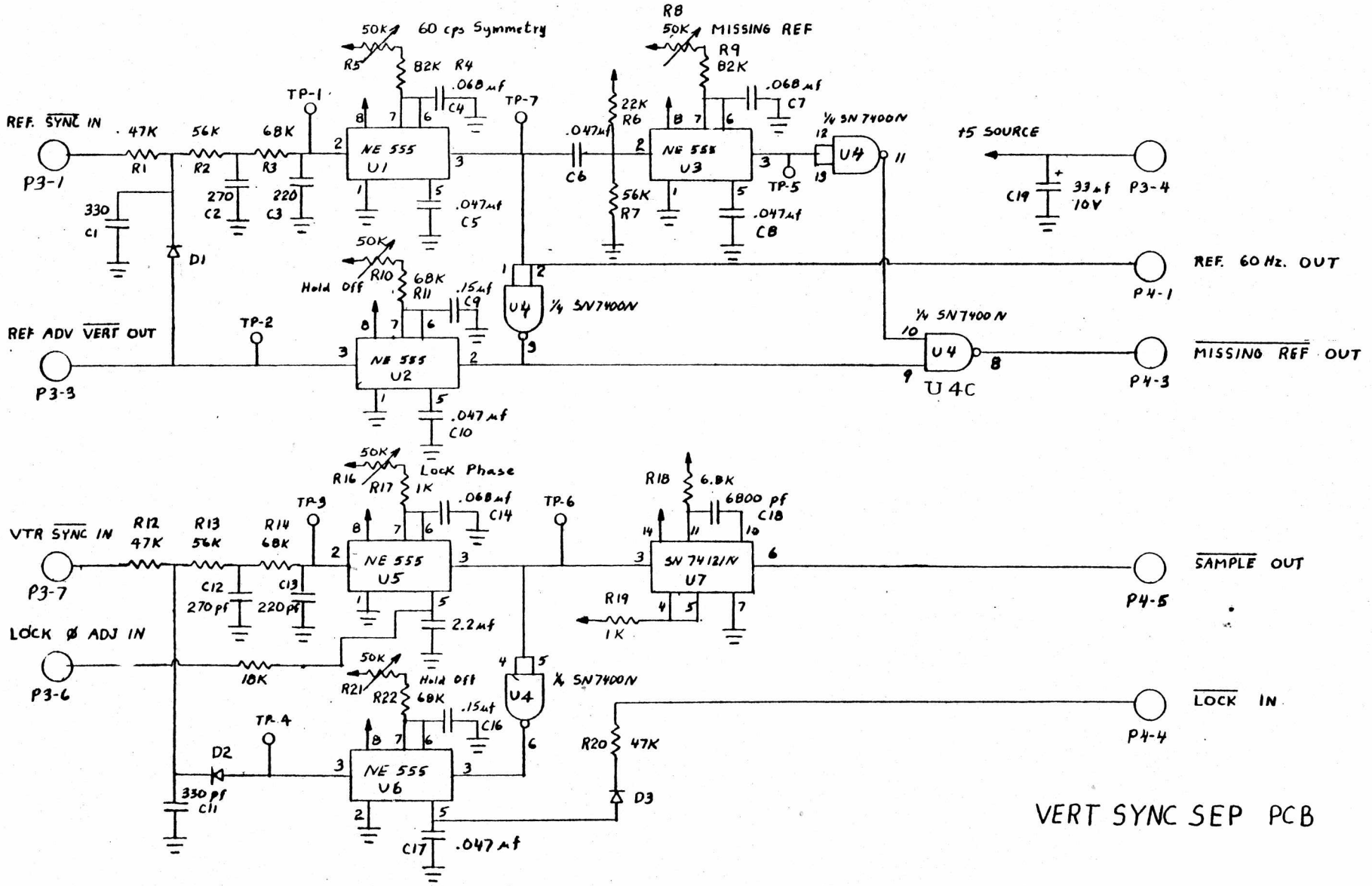


2) Cut off pin #11

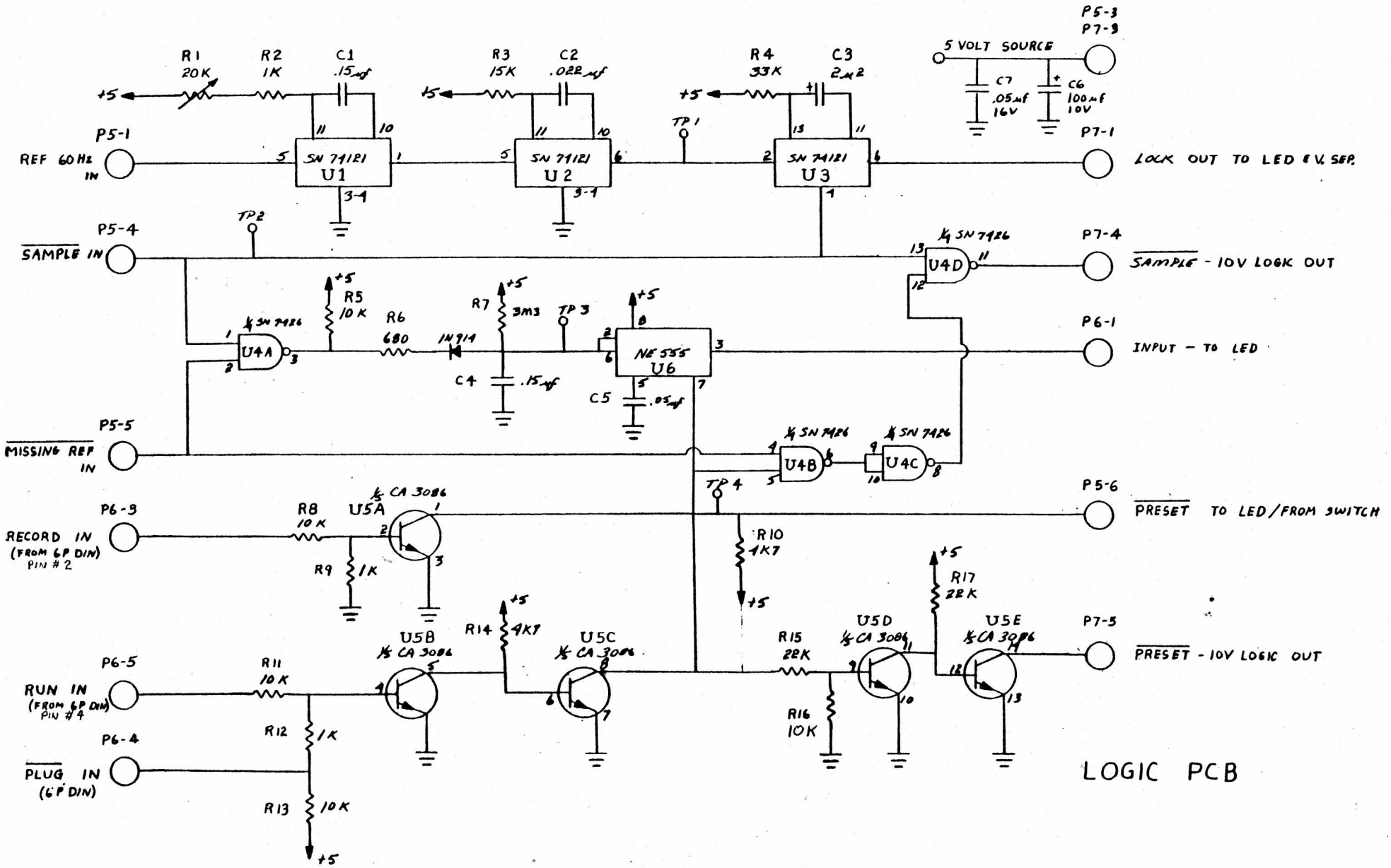
The schematic then becomes:

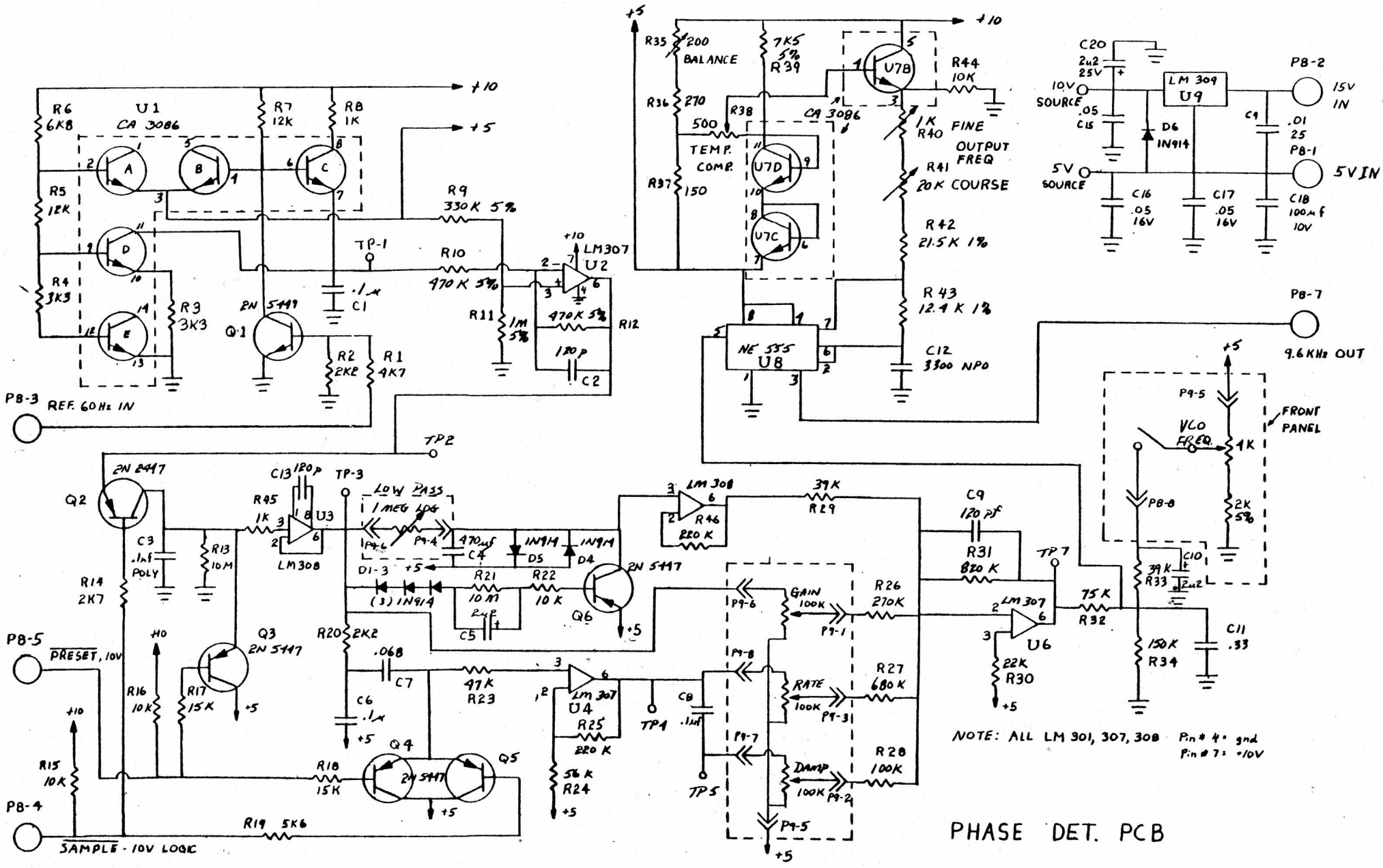


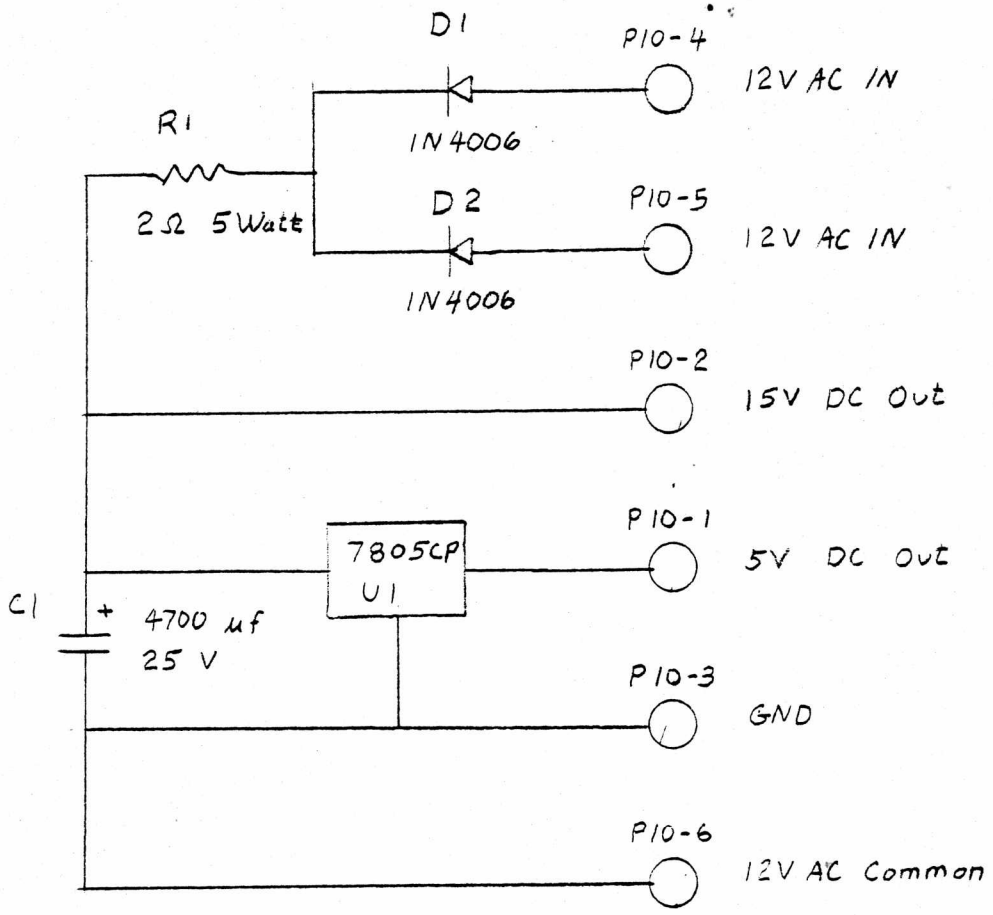

P1-2
5V SOURCE
C17
C18
C19
100 uf 10 V
100 uf 10V
.05 uf 16V
P1-1
REF. VIDEO
C1
2u2
R1
22K
R3
10K
R2
33K
R4
1K
C2
33 uf
R6
3K3
R7
1K5
C3
33 uf
C4
.47
R8
1K5
R9
1K7
R10
3K9
U2A
U2B
U2C
U2D
U2E
1/4 CA 3086
C5
.001
R11
3m3
R12
470
R13
680
R14
100K
C6
2u2
R15
150
R16
10K
R17
10K
TP1
TP2
U3A
U3B
U3C
U3D
U3E
U3F
1/6 SN 7405N
R18
1K
R19
1K
R20
1K
P2-1
SYNC OUT
P2-2
SYNC OUT
P2-3
% CLAMP
P2-4
REF VIDEO TO FRONT PANEL
1k
R5
U1A
U1B
U1D
U1E
C9
2u2
R23
1K
R24
220
C7
1nf
R21
390
C8
1nf
R22
3K9
TP3
R26
330
R27
1K
C10
.47
P1-6
VTR VIDEO
P2-7
TO FRONT PANEL
DUPLICATE OF ABOVE CIRCUIT ON SAME PCB.
P2-6
VTR SYNC OUT
P2-8
VTR SYNC OUT
P1-5
+5 VTR SYNC SEP
C13
C14
C15
C16
100 uf 10V
.05 uf 16V
100 uf 10V
.05 uf 16V
% CLAMP
R28
1K
Q1
2N 5449
R29
2K7
R30
220
2N5449
Q2
C12
500 uf
R31
68
P1-3
MONITOR
C11
2u2
VIDEO FROM U1, PIN 9 VTR VIDEO
P2-5
% CLAMP FROM VIDEO REF THRU MON SELECT SWITCH
SYNC SEP PCB



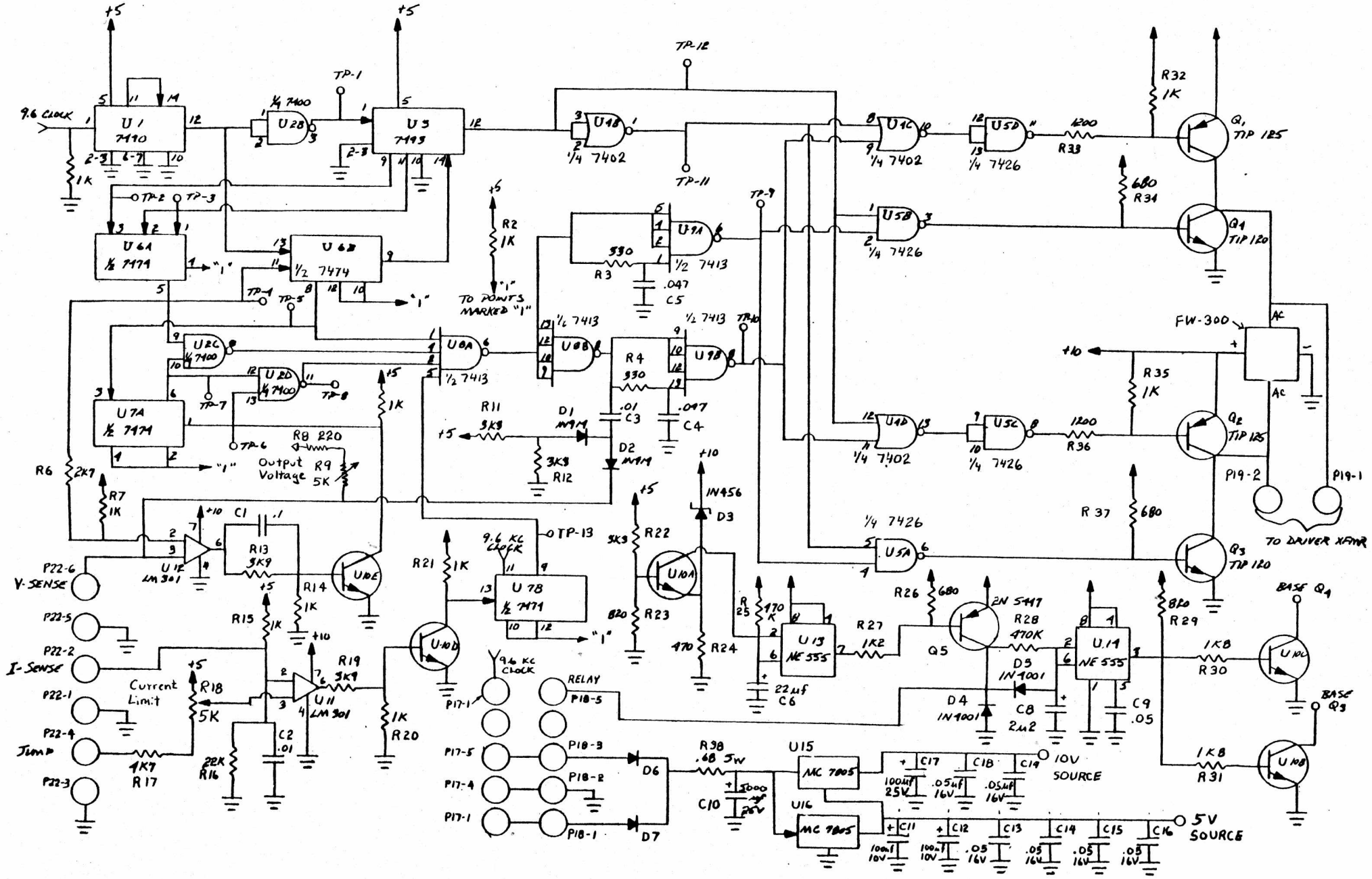
VERT SYNC SEP PCB


P5-3
P7-3
5 VOLT SOURCE
R1
20K
R2
1K
C1
.15 mf
R3
15K
C2
.022 mf
R4
33K
C3
2.2
C7
.05mf
16V
C6
100mf
10V
P5-1
REF 60Hz IN
SN 74121
U1
SN 74121
U2
TP1
SN 74121
U3
P7-1
LOCK OUT TO LED & V. SEP.
P5-4
SAMPLE IN
TP2
1/4 SN 7426
U4D
P7-4
SAMPLE - 10V LOGIC OUT
R5
10K
R6
680
1N914
R7
3M3
TP3
NE 555
U6
C4
.15 mf
C5
.05 mf
1/4 SN 7426
U4A
P6-1
INPUT - TO LED
P5-5
MISSING REF IN
1/4 SN 7426
U4B
1/4 SN 7426
U4C
TP4
P5-6
PRESET TO LED/FROM SWITCH
P6-3
RECORD IN
(FROM 6P DIN)
PIN # 2
R8
10K
1/4 CA 3086
U5A
R9
1K
R10
4K7
R17
22K
P6-5
RUN IN
(FROM 6P DIN)
PIN # 4
R11
10K
U5B
1/4 CA 3086
R14
4K7
U5C
1/4 CA 3086
R15
22K
U5D
1/4 CA 3086
U5E
1/4 CA 3086
P7-5
PRESET - 10V LOGIC OUT
R16
10K
P6-4
PLUG IN
(6P DIN)
R12
1K
R13
10K
LOGIC PCB

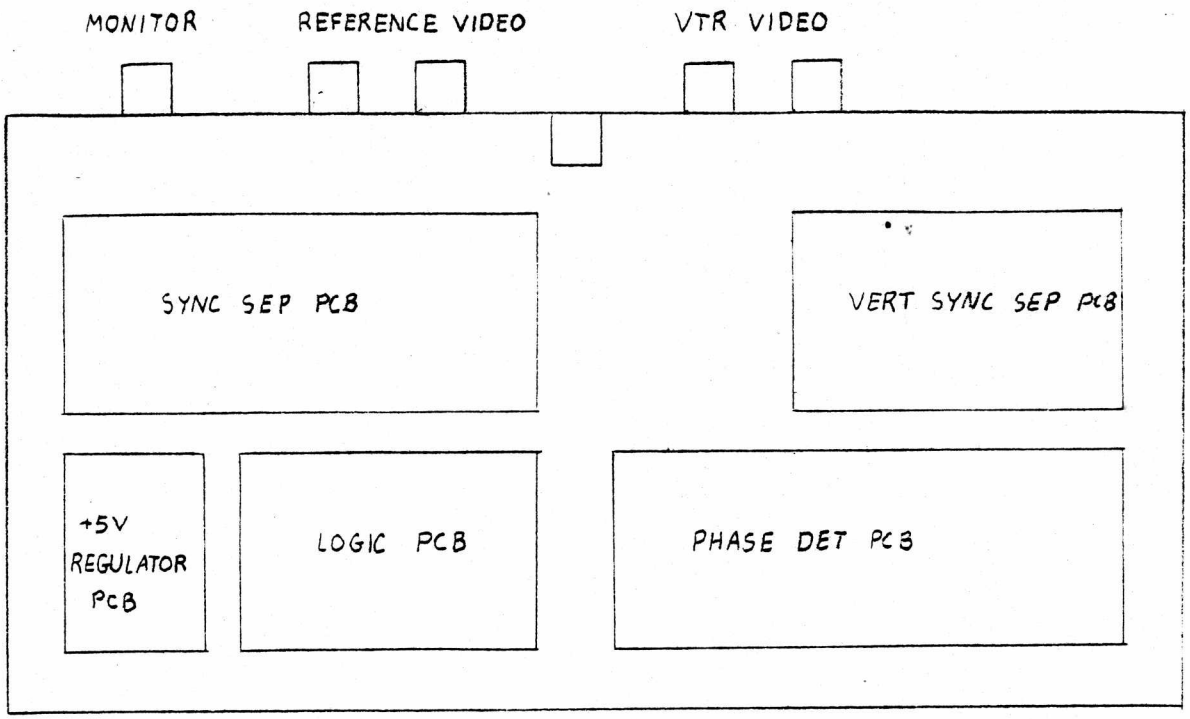

+10
+5
R6 6K8
U1 CA 3086
R7 12K
R8 1K
R5 12K
R4 3K3
R3 3K3
R9 330K 5%
TP-1
R10 470K 5%
C1 .1µ
2N 5449 Q1
R11 1M 5%
LM307 U2
470K 5% R12
120P C2
R2 2K2
R1 4K7
P8-3 REF. 60Hz IN
TP2
R35 200 BALANCE
R36 270
R37 150
500 R38
7K5 5% R39
TEMP. COMP.
U7B
U7D
U7C
CA 3086
R44 10K
1K R40 FINE
OUTPUT FREQ
R41 20K COURSE
R42 21.5K 1%
R43 12.4K 1%
NE 555 U8
C12 3300 NPO
C20 2µ2 25V
10V SOURCE
.05 C15
5V SOURCE
C16 .05 16V
C17 .05 16V
LM 309 U9
D6 IN914
C9 .01 25
C18 100µf 10V
P8-2 15V IN
P8-1 5V IN
P8-7 9.6KHz OUT
P9-5
VCO FREQ.
1K
2K 5%
FRONT PANEL
P8-8
39K R33
C10 2µ2
150K R34
C11 .33
2N 2447 Q2
C13 120P
TP-3
R45 1K
LM308 U3
LOW PASS 1 MEG LOG
P9-4
P9-6
470µf C4
1N914 D5
1N914 D4
D1-3
(3) 1N914
R21 10M
R22 10K
2N 5447 Q6
LM 308 R46 220K
39K R29
C9 120 pf
R31 820K
TP 7
LM 307 U6
75K R32
22K R30
C3 .1µf POLY
R13 10M
R14 2K7
P8-5 PRESET, 10V
HO
Q3 2N 5447
R16 10K
R17 15K
R20 2K2
.068 C7
C6 .1µ
47K R23
LM 307 U4
R25 220K
56K R24
TP4
C8 .1µf
TP5
GAIN 100K
RATE 100K
DAMP 100K
R26 270K
R27 680K
R28 100K
P9-1
P9-3
P9-2
P9-7
P9-8
P9-6
Q4
Q5
R18 15K
R19 5K6
P8-4
R15 10K
SAMPLE - 10V LOGIC
NOTE: ALL LM 301, 307, 308 Pin # 4 = gnd Pin # 7 = +10V
PHASE DET. PCB



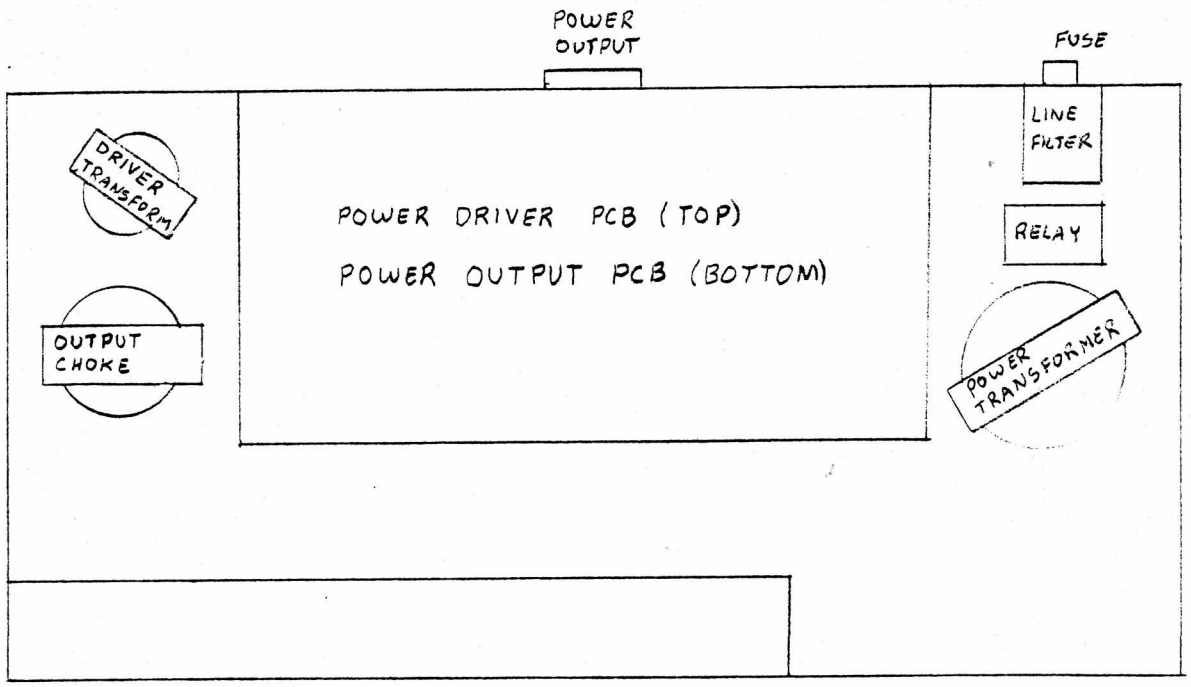
5 VOLT REGULATOR PCB



POWER DRIVER PCB

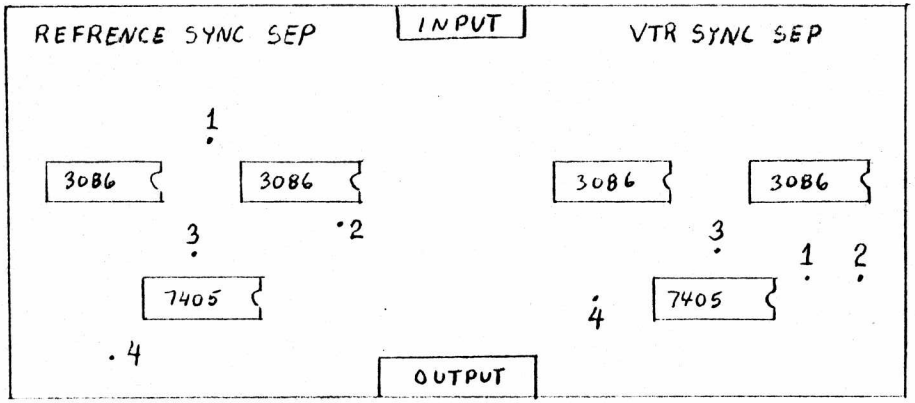


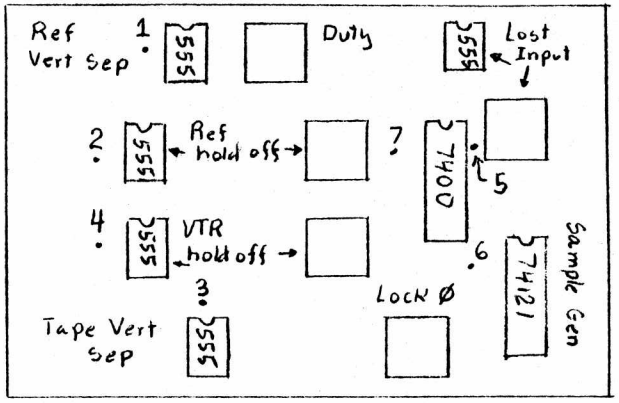
BOTTOM VIEW

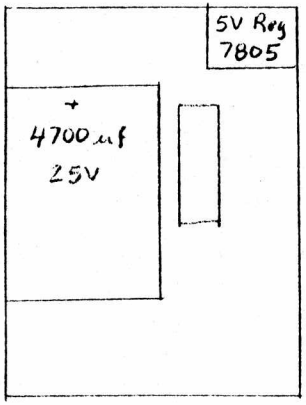


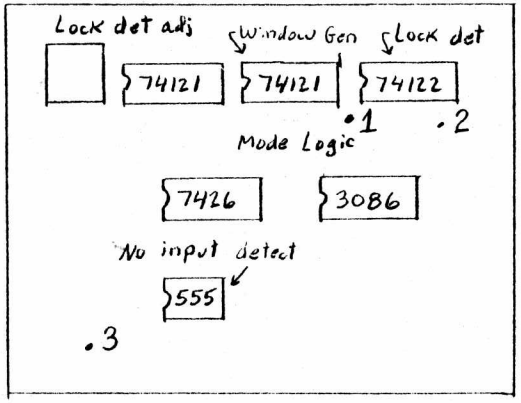
TOP VIEW

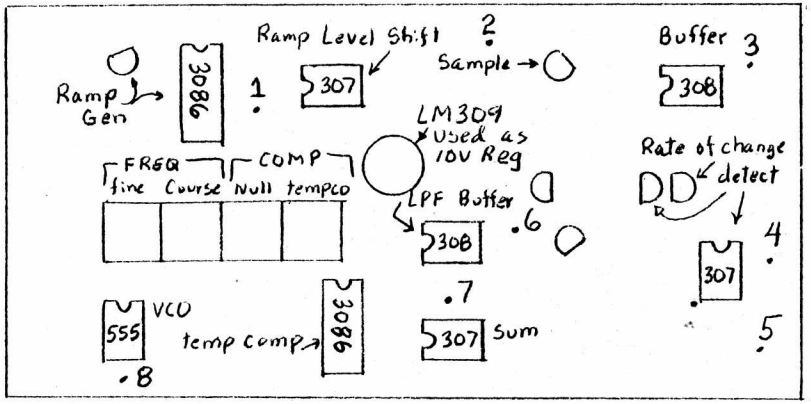
PCB LOCATION





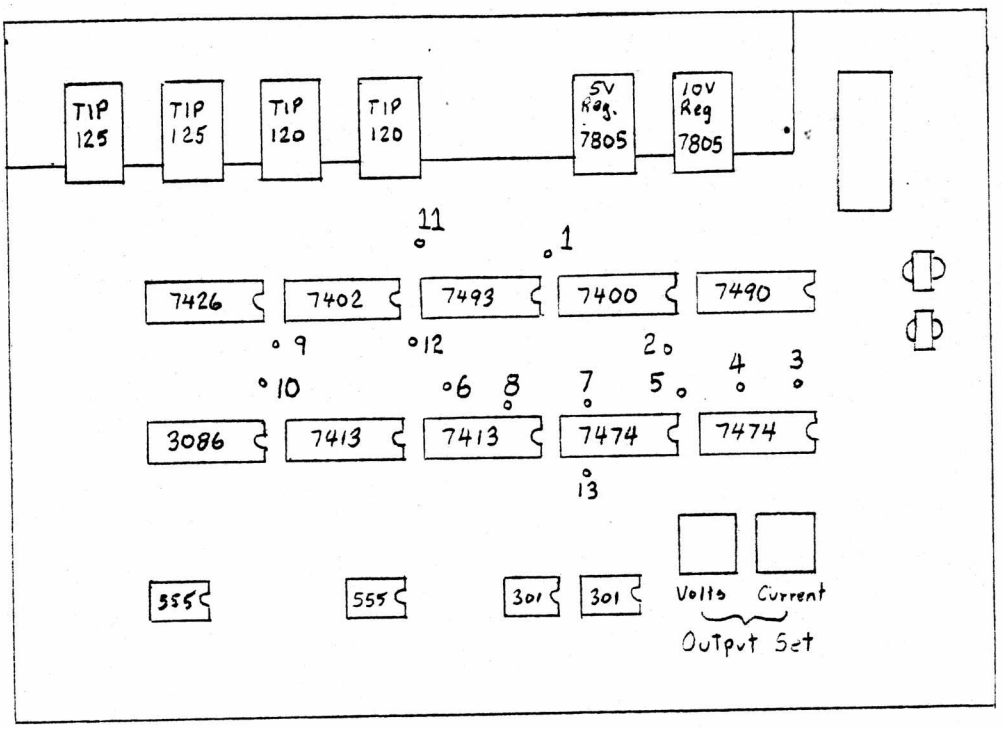




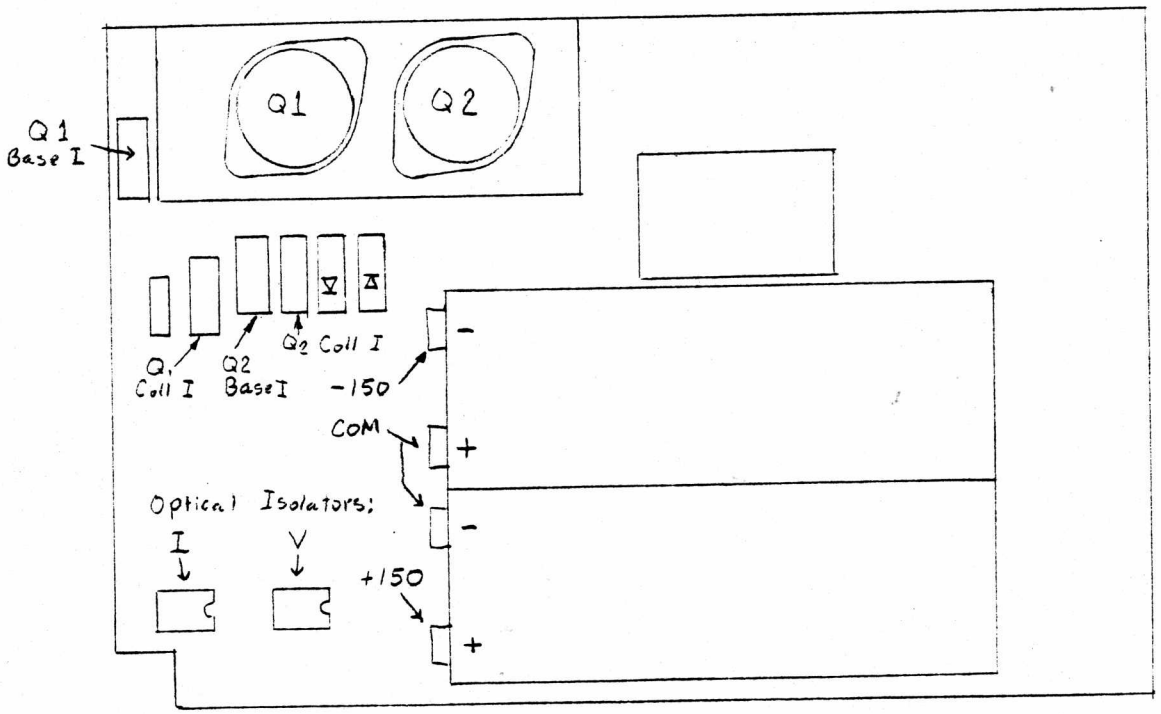


ADJUSTMENTS & TEST POINTS

Bottom of VS-1000



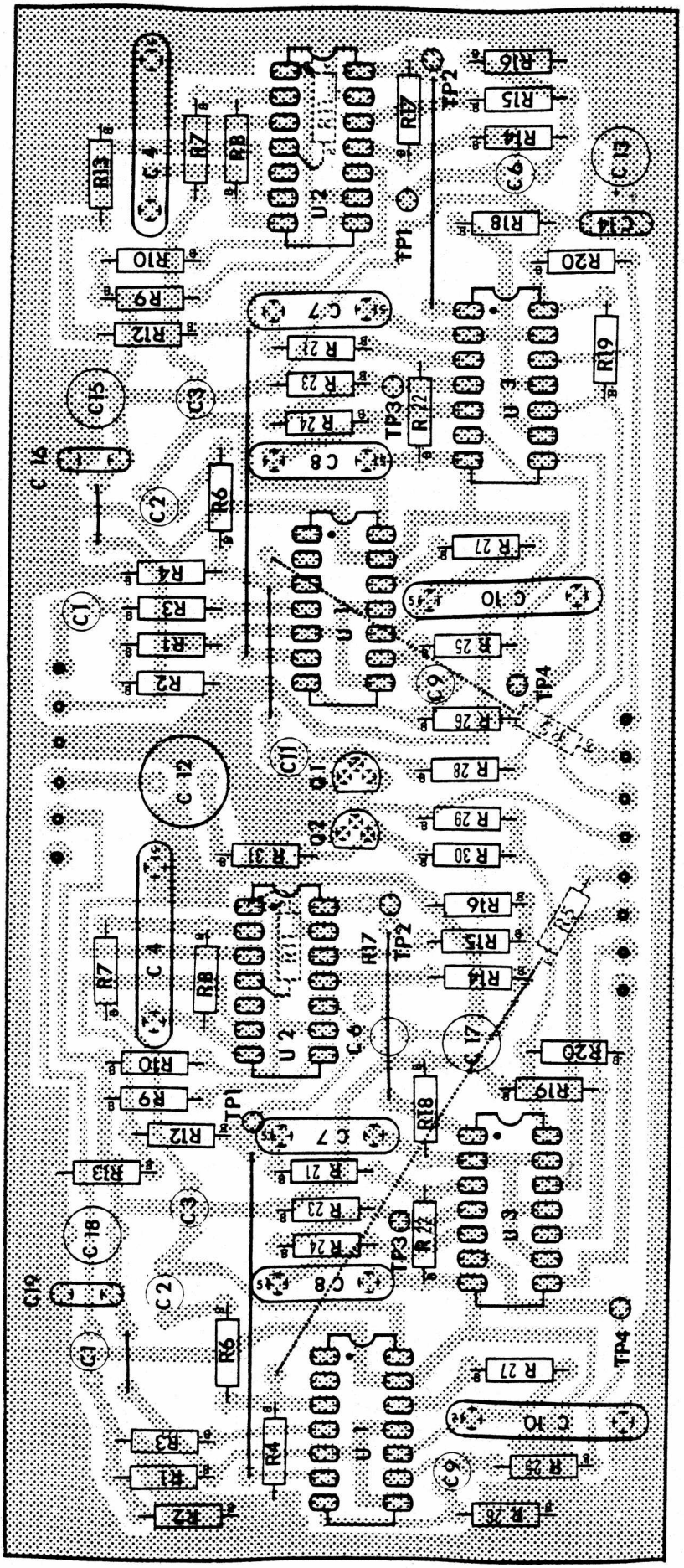
POWER DRIVER PCB



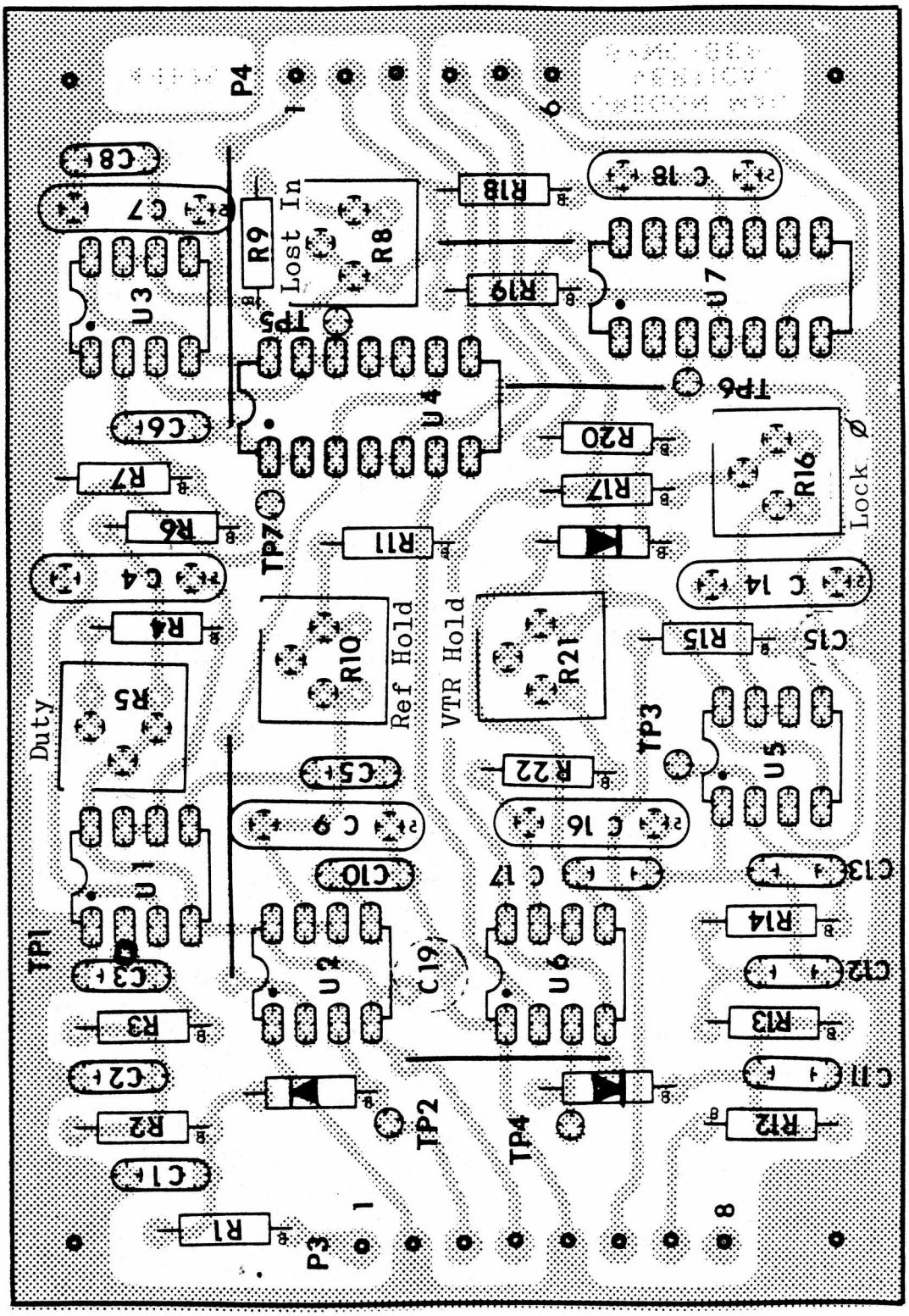
POWER OUT PCB

ADJUSTMENTS & TEST POINTS

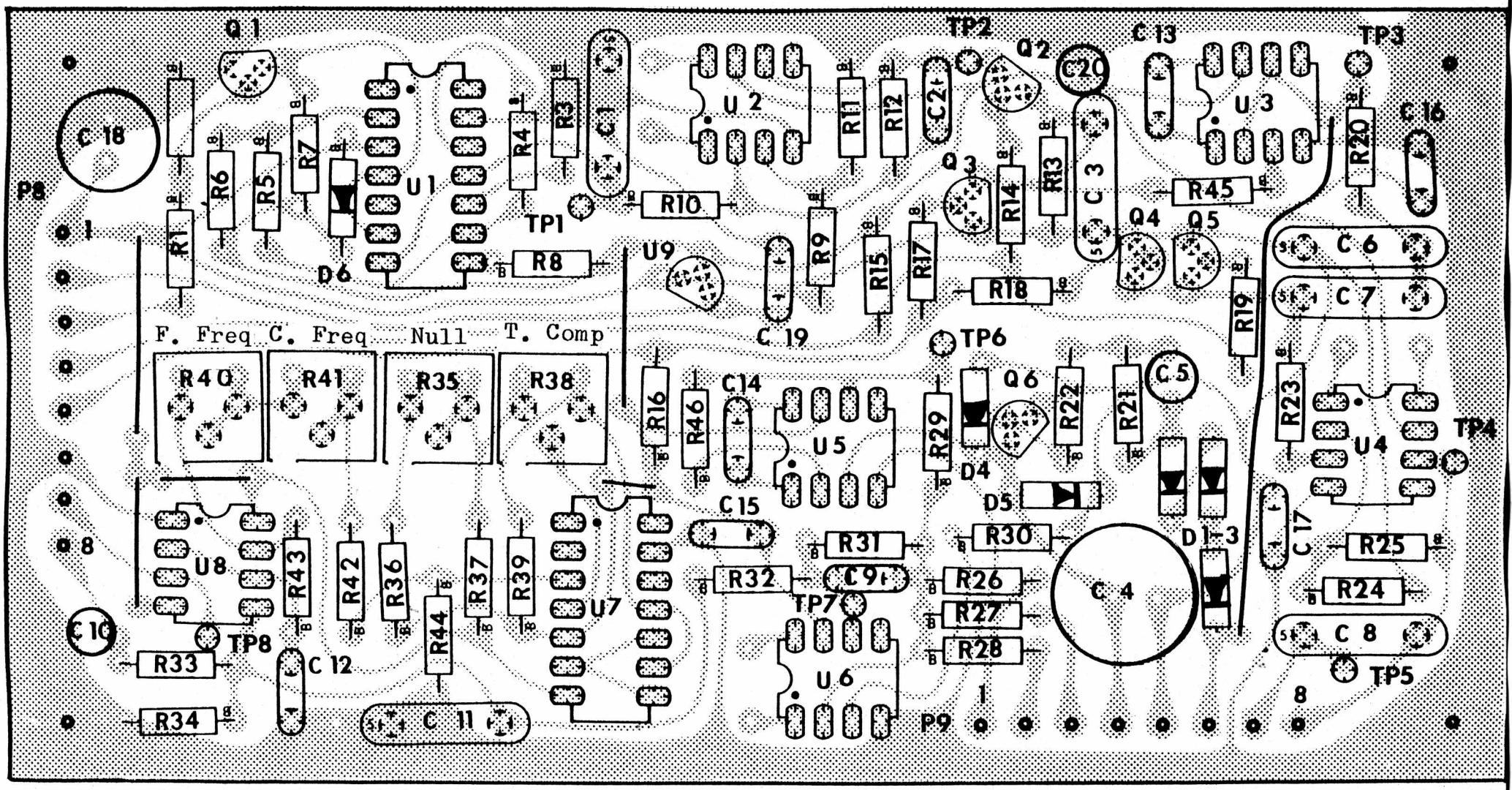
Top of VS-1000


R16
R15
R14
C6
C13
C14
R18
R20
R19
U3
TP2
TP1
R17
U2
R13
C4
R7
R8
R10
R9
R12
C7
R21
R23
R24
C8
TP3
R22
C15
C3
C16
C2
R6
R4
R3
R1
R2
C1
C10
R25
C9
TP4
R26
R28
R29
R30
C12
C11
Q1
Q2
R31
R5
C17
C18
C19

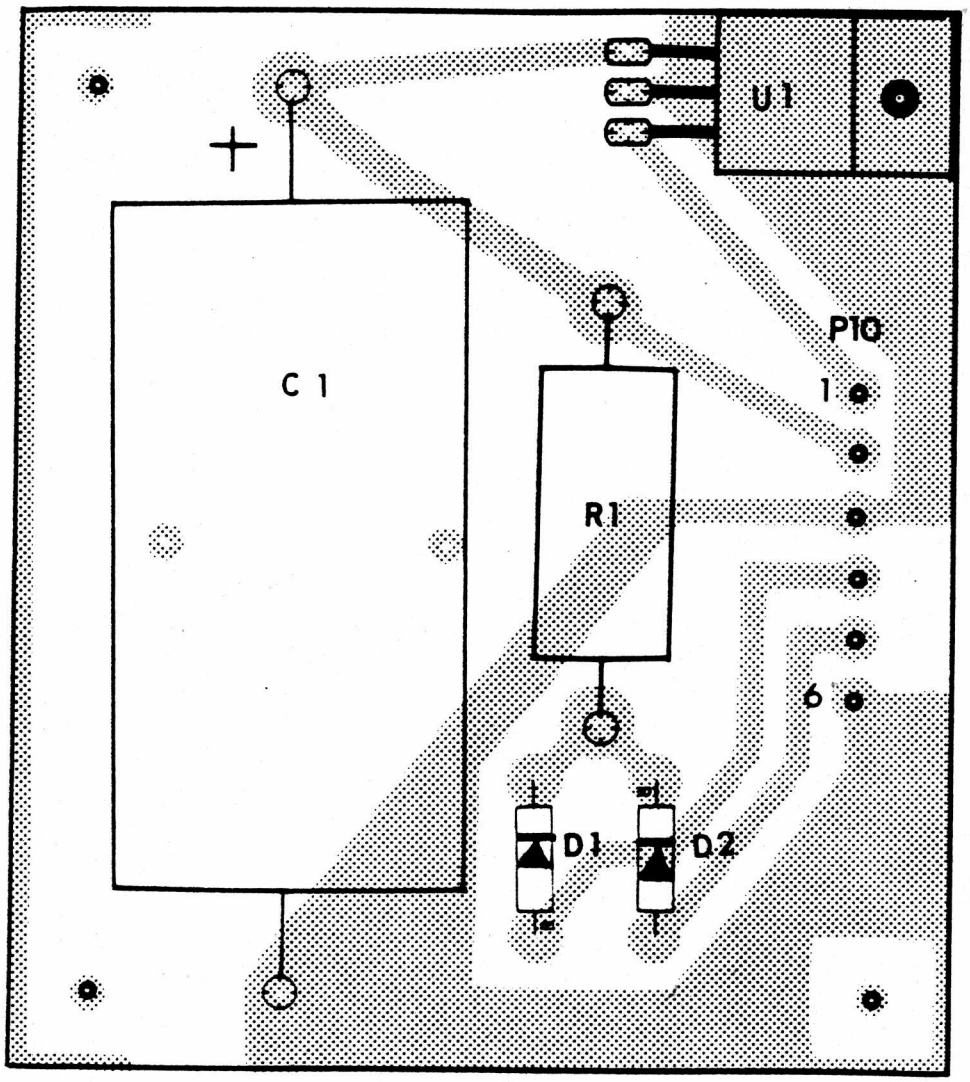
SYNC SEP PCB



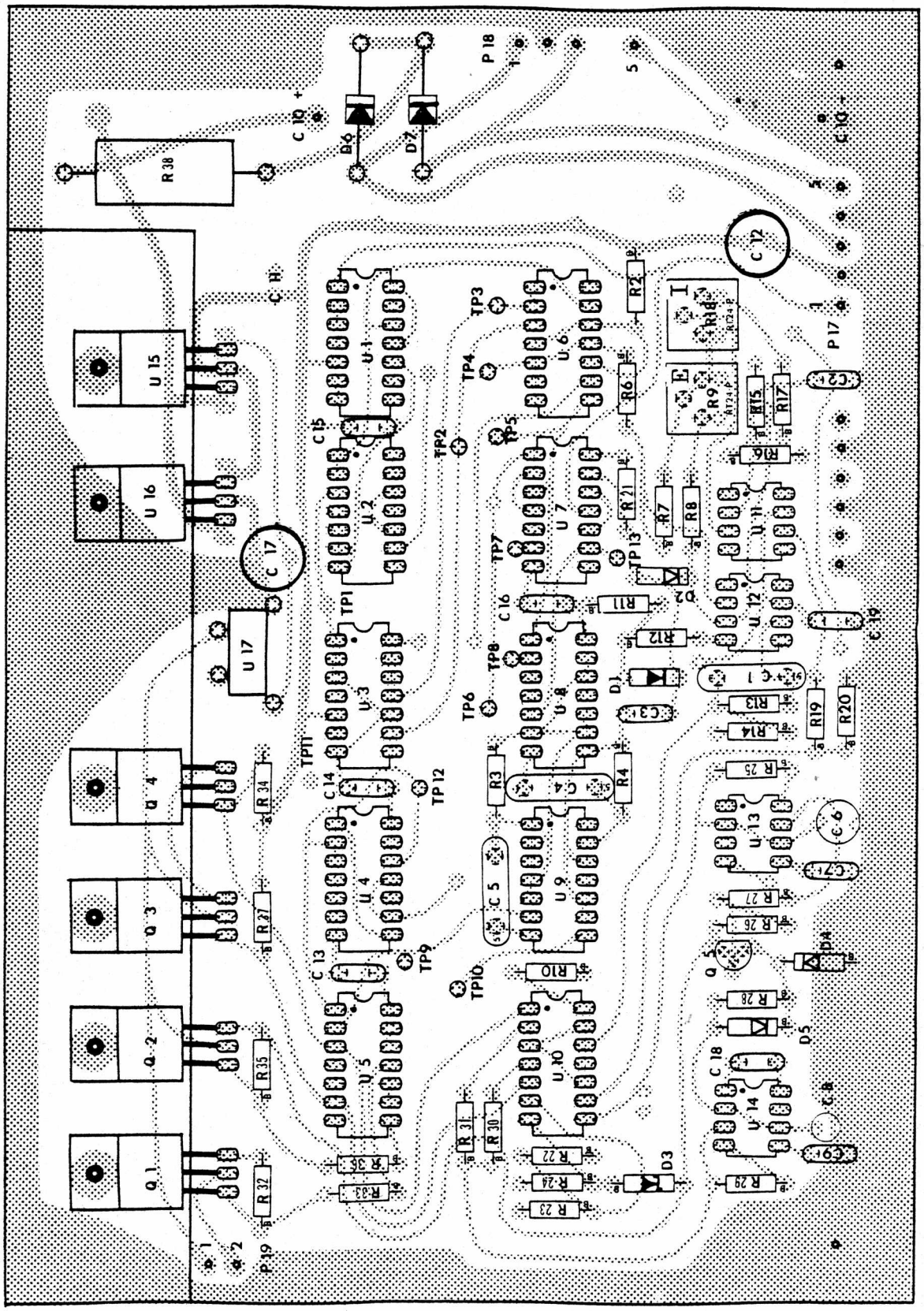
VERT SYNC SEP PCB



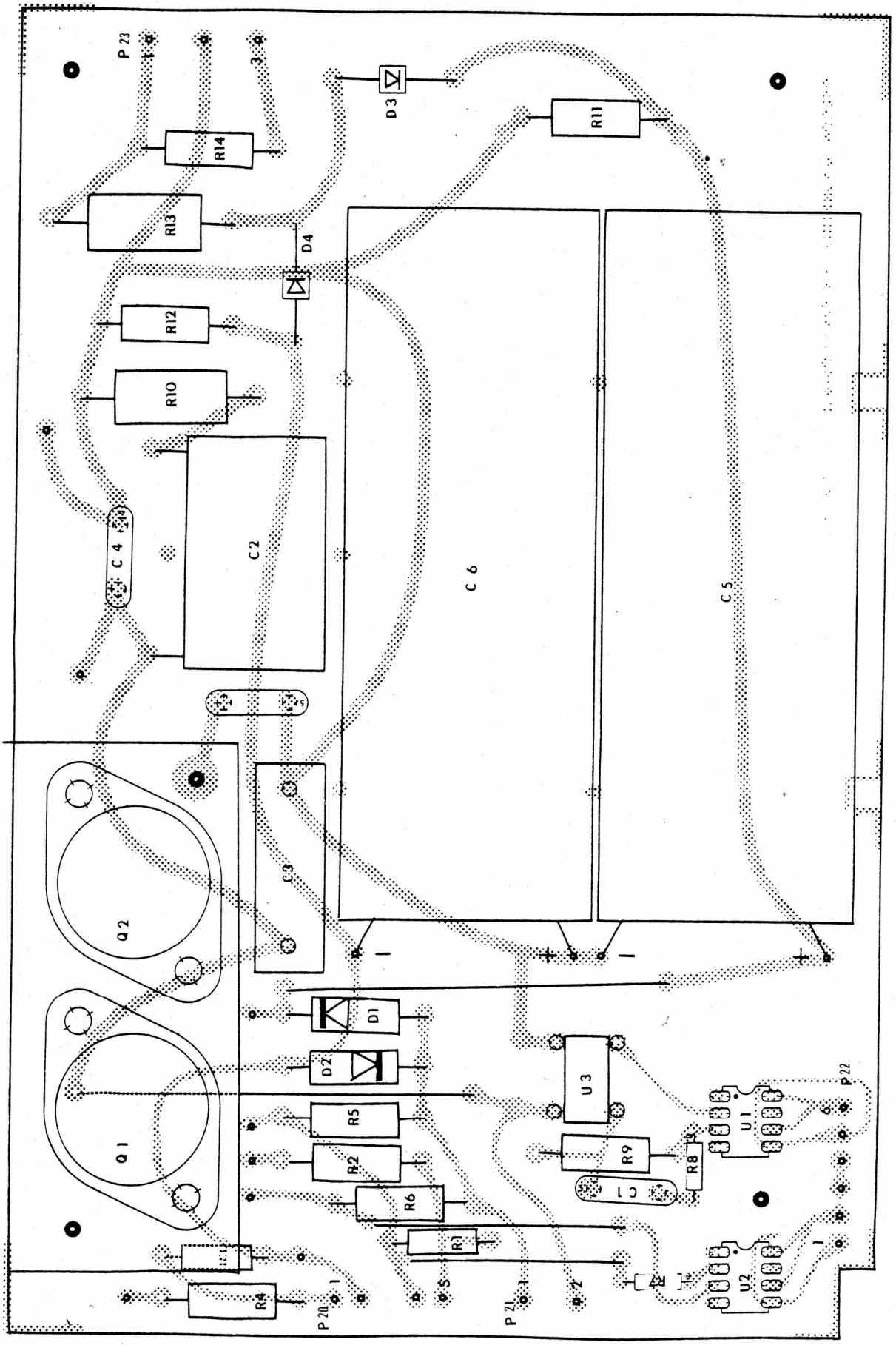
PHASE, DET PCB



5V REGULATOR PCB



POWER DRIVER PCB



POWER OUTPUT PCB